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BOOKS/CONFERENCE INDEX 2018-2019

3.3.2 Number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during 2018-2019

Sl. No.	Name of the teacher	Title of the book/chapters published	Title of the paper	Title of the proceedings of the conference	Name of the conference	National / International	Calendar Year of publication	ISBN number of the proceeding	Affiliating Institute at the time of publication	Name of the publisher
1	Neenu Sebastian		A Comparative Study of Performance and Security Issues of Public Key Cryptography and Symmetric Key Cryptography in Reversible Data Hiding	Advances in Intelligent Systems and Computing book series (AISC,volume 939)	IBICA 2018: Innovations in Bio-Inspired Computing and Applications pp 406–412	International	May 2019	978-3-030-16681-6	SCMS School of Engineering and Technology, Ernakulam, India	Springer Link
2	Dr.Varun G Menon		Distributed Big Data Analytics in the Internet of Signals	IEEE Xplore	2018 International Conference on System Modeling & Advancement in Research Trends (SMART)	International	November 2018	978-1-5386-6369-1	SCMS School of Engineering and Technology, Ernakulam, India	IEEE
3	Dr.Varun G Menon		A Top-Up Design for PAL to VGA Conversion in Real Time Video Processing System	IEEE Xplore	2018 International Symposium on Advanced Electrical and Communication Technologies (ISAECT)	International	July 2018	ISBN:978-1-5386-7329-4	SCMS School of Engineering and Technology, Ernakulam, India	IEEE
4	Dr.Ratish Menon	ISOLA Kerala Chapter	Multicriteria ranking of the best management practices for flood reduction in Kochi city, India	ISOLA Kerala Chapter	13th ISOLA Annual Conference-Reimagining Landscapes, Kochi-February 15&16, 2019	International	February 2019		SCMS Water Institute, SCMS School of Engineering and Technology,	Indian Society of Landscape Architects
Total number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during 2018-2019										4

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A Comparative Study of Performance and Security Issues of Public Key Cryptography and Symmetric Key Cryptography in Reversible Dat

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2018)

S. Anagha, Neenu Sebastian & K. Rosebell Paul

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Distributed Big Data Analytics in the Internet of Signals

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***Abstract*—Internet of Things (IoT) is a network of ubiquitous devices that are capable of computation and communication over the Internet. These 'things' or devices continuously generate data over the internet and often communicate their data with a central server. Data circulated in this network can be either a control signal or a time dependent signal. The fusion center transforms the collective data from spatially distributed sensing nodes into useful information known as the analytic. This research paper examines the computation of linear and non-linear data analytic in a distributed IoT network. IoT sensors are required to save battery and bandwidth. Further, the constraints in the computation and communication functionalities are highlighted, and also directions towards solving gaps in the present IoT standards are enlisted.**

Keywords: Analytics, Big Data, Communication, Distributed, IoT, Internet of Signals, Sensors

I. Introduction

The Internet of Things is envisioned to be a key technology driver in the future [1-8]. The IoT framework is laid on the foundations of the Internet, which is a global network of computers. Mobile devices have revolutionized the way we interact with data. In future these devices can sense and report real-time data to Internet servers, which provide useful analytics/information. IoT standards are evolving to address some of the challenges in health-care, transport, citizen services, environmental pollution, power distribution and lighting, infrastructure management. These developments lead to enable the global vision of smart cities, and towards easier and reliable technology that are accessible to all [9]. It would certainly improve the quality of human life and generate positive movements in world's economy.

The wide coverage of topics ensembles the ideas from varied engineering streams to address some of the current challenges of climate change and pollution. IoT paradigm is laid on the three primary functionalities of *sensing*, *management* and *feedback*. The network consists of millions of everyday `things' (for e.g. devices) that are equipped with sensing, computation and communication capabilities. Each functionality is performed through the protocol stack with the assistance of the central node. Sensors are involved in the sensing of physical layer signals and storing it for future computation and communication. This is one of the most researched areas in recent times. Sensing, collection and storage of this big data [10-12] is a challenging task and involves concerns in security also. Most common sensing data (or signals) include temperature, pressure, humidity, energy, load, proximity and activity.

Sensed data can be used to derive signals which can be broadly classified as:

- **Real-Time Signals/Data**: Sensor nodes report the observed signal to the central server
- **Data used for Commanding**: Sensor nodes transmit commands/instructions to the peer nodes.

Our focus here is on the former where the server (fusion node) requires to derive a function over the reported data. Figure 1 elaborates the concept of Smart City with automated homes enabled via Internet of Things (IoT). The smart homes adjust lights, connect and manage electronic gadgets, monitor preservation of food. The central server in the data center (cloud) is connected via the home Internet service provider.

The second functionality of management refers to the control of sensors, monitoring of sensors, network state (whether ON/OFF), and actuation of various network elements. Feedback is a necessary functionality of IoT, as it enables the update of the network assigned jobs, recovery of failed nodes and adaptation of various network related algorithms. The protocol stack of the IoT network enables efficient end-to-end reliable communication between any nodes. The various levels of the stack can be broadly diversified as:

- Control
- Communication
- Networking
- Sensing
- Actuation

Fig. 1: A Smart City with Automated Homes

In the present IoT standards, the signal processing domain is less emphasized. The only mention of DSP occurs in the aspects of sampling and quantization at the sensor. The mention of the signal processing here refers to the approximation or compression perspective. Broadly data and signal analytics can be categorized as:

- Linear
- Non-Linear

Linear analytics are functions over the data that satisfy the superposition principle. Most common linear data includes addition, average, XOR, median etc. The idea of linearity over data can be elucidated using the example of two distributed temperature sensors as show in Figure 2. In figure 2, temperature sensing nodes S1 and S2 monitor the real time temperature data at two geographically separated locations. The central server F, needs to determine the average temperature in the region. Here the average temperature is the sum of the individual average data's.

The linear analytic computation will at most consists of a few additions in the respective representation domains [13]. In large networks, linear analytics can be performed over the intermediate compute nodes. This dramatically reduces the computation overhead at the fusion node. By performing linear network coding the computation complexity can be reduced to a linear scaling factor [14]. In a majority of linear computation over networks, only scalar data is required to be considered.

A non-linear function does not satisfy the superposition principle. Some examples include functions such as the min, max and the histogram. The non-linear nature of the computation is challenging, since it requires a chunk of vector data to be transmitted over the finite bandwidth channel. The example of a nonlinear data is that of a Holter monitor which is used to obtain a 24 hr Electrocardiogram. Real-time ECG measurements consume large amounts of storage of data collected from electrodes placed at multiple locations. For through analysis by doctor, the ECG data has to be converted to suitable histogram. Reporting this data over long distances costs channel bandwidth and delay if direct transmission is employed. Thus, in practice a good representation of the signal needs to be applied.

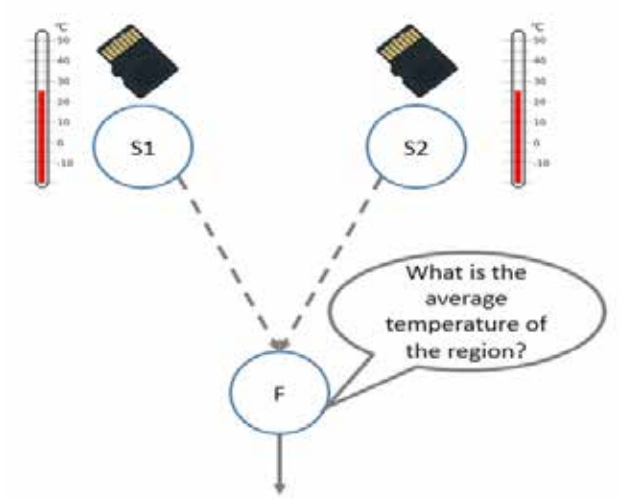

Fig. 2: Two Temperature Sensing Nodes, S1 and S2 Monitor the Real Time Temperature Data at Two Geographically Separated Locations

II. Distributed System Description

A distributed system is one that consists of independent peripheral nodes located at spatially separated regions. The network nodes are non-cooperative in nature and are capable of performing real-time storage and computation. The sensing capability in each node along with its memory enables them to record the observed data. Each of the recorded data is to be conveyed to the fusion node by using efficient data (or signal) representation schemes.

Some of the well-known schemes in source coding such as Huffman coding, Run length coding, Lempel-Ziv coding. Alternatively, in the case of signals commonly used representations include the Fourier and the Wavelet basis. The choice of the coefficients to be transmitted is decided by the analytic that is to be computed. For instance the computation of the average temperature at separate sensors is possible if individual sensors report their respective observed averages [13]. In terms of the Fourier representation this corresponds to the DC (zero frequency) coefficient.

A. How Big is the Data?

Consider a city having a million plus population. Around 10% (patients) of the population suffer from heart related diseases. The city health department initiates a scheme to collect and analyse the ECG data that has to be reported to the heart specialists in the locality. Each diagnosed patient is provided with a "smart" Holter monitor that has 7 electrodes. The device picks up the bio-signal at the rate one sample per minute. If the raw signal representation takes 1Kb/sample, by the end of each day, the central server needs to deal with 120 GB. The complete scenario is presented in figure 3.

This type of situation is true in all major applications of IoT. Internet of connected vehicles [15] and vehicular fog networks [16-17] is yet another application where the

collection, analysis and storage of very large amount of data is required. Most of the modern applications thus have to manage enormous data. Mining of required data from this big data is a big challenge.

B. Communication in Internet of Things

The simplest communication in IoT occurs between the devices or the 'things'. These smart devices communicate over different types of network such as Wi-Fi, Bluetooth, ZigBee or Internet. These devices are manufactured by different vendors and use a common communication protocol to send and receive their messages over the network.

Figure 4 shows the communication between two devices connected via a wireless network. This communication model is mainly used in home automation systems that usually involve low data transfer rate.

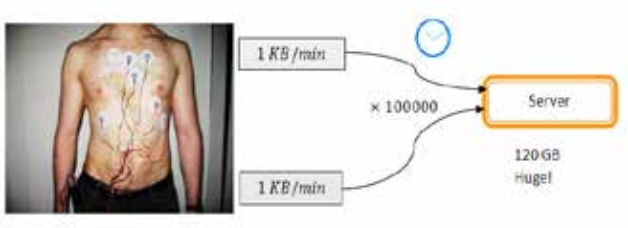

Fig. 3: Scenario of Big Data

Fig. 4: Device to Device Communication

The next bigger communication happens with device to cloud model [18] in which the devices are connected directly to an Internet cloud service to exchange data and control the traffic. With this type of communication users can obtain remote access to their devices via a smart phone or a Web Interface. The Samsung Smart TV uses this technology to transmit the user viewing information to Samsung for analysis and for helping with other advanced features such as interactive voice recognition. Figure 5 shows the big picture of Internet of Things Network. Here data from devices such as sensors, CCTV camera's, reaches a central cloud server after passing through the Internet. With millions of laptops and smart phones connected to the internet, any user can obtain this data for analysis and other purposes.

C. Protocol Stack Description

In IoT the protocol stack consists of control, communication, networking, sensing and actuation. In the control layer, commanding data is generated (or decoded). It includes actions such as turning ON/OFF the sensors, enabling sleep mode or information corresponding to sampling rate/quantization. The communication layer handles inter node communication through the physical channel (with channel noise). It covers schemes involving power control rate adaptation, channel coding and error correction. Energy harvesting schemes and models are developed at the sensors, since they have to stay alive for several months. The common harvesting sources for sensors include solar power, piezo-electric (body networks), bio-electric and wind power. Recent developments in IOT physical layer communication design involve inclusion of these energy harvesting models for optimizing the power utilization and maximizing the data rate. Physical layer security is an emerging area, which overcomes many drawbacks of the network layer security [19]. Privacy and security aspects of the IoT network needs to be relooked from the physical security perspective since it offers better reliability and optimized power utilization.

Fig. 5: Internet of Things Network

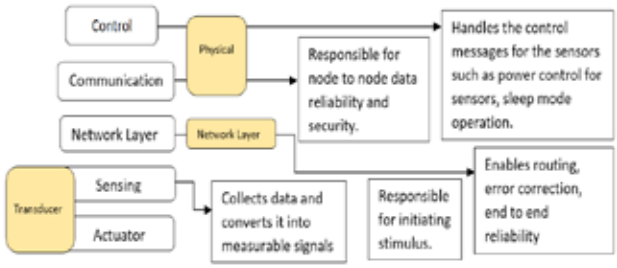

Fig. 6: Various Layers of the Protocol Stack its Functionalities

III. Big Data Analytics

Big data analytics [22] deals with the measurement of data that has come from distributed sensor nodes spread geographically. The linear data analytics can be represented as linear function computed over the data.

$$\Theta_{linear} = A\,D,$$

Where A is the coefficient matrix and D is the data representation matrix. For the average temperature between two temperature nodes the coefficient matrix is [½,½] and the data matrix is a 2 x 1 matrix consisting of the DC

coefficients of the Fourier representation. We can also see that in the case of more than two sensors the analytic computation can be performed by the intermediate nodes. Node T_1 sends its coefficient to T_2, where it fuses its own temperature. Then a similar fusion is performed at T_3 and finally updated at F.

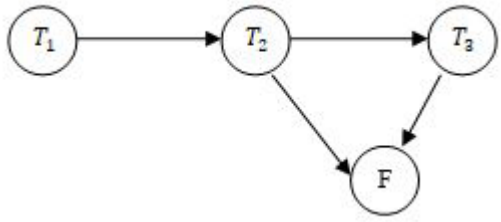

Fig. 7: A Non-Meshed Sensor Placement, with Intermediate Nodes Performing Fusion Computation. Here each Node Computes a Linear Function of the Present Data at the Current Node and the Incoming Flow

Non-linear fusion computation is less dealt with in the upcoming IoT standards. The fusion node here needs to derive a non-linear function of the data. The use cases of such analytics are in the context of determination of the spiking of the ECG recorded data. The peak determination in ECG signal includes the functions like maximum and the gradient. Traditional signal processing approaches like the cost minimization using least squares can be performed based on some statistical data assumptions. The unconstrained minimum mean square cost is represented as:

$$\Theta_{MMSE} = \min_{\tilde{\Theta}} \mathbb{E}\left[\left(\tilde{\Theta} - \Theta\right)^2\right],$$

Where $\tilde{\Theta}$ corresponds to the estimate of the analytic and Θ is the true analytic (in most cases this is a constant). The representation of the analytic demands some compression to be applied, i.e. the estimated parameter is transmitted using a few coefficients through the communication channel.

IV. Challenges and Future Research Directions

This section discusses the challenges and issues existing in analytics of big data collected from IoT devices and also presents future research directions for researchers.

A. Security and Privacy

The most important issue faced by researchers worldwide is in the security of methods used in data collection and storage [20-21]. As the amount of data is huge, essential care should be taken to protect the data from misuse. Selection of appropriate data collection methods is very important. Trusted data collection centres play a vital role in ensuring the security of data. Security and privacy of the devices involved in data transfer is a highly researched area. Further intense research has been carried out to secure the data that is being transferred from the source to the destination device via the intermediate devices. A large number of open research problems still exist in IoT security.

B. Storage of Data

With enormous amount of data generated every second, one of the major challenges is in proper storage. With the amount of data increasing day by day, scalability of storage systems is another major concern. Huge data centres dedicated for storage often leads to high cost in the deployment of the IoT system. Many researches have been directed at improving the storage capabilities of the IoT devices.

C. Efficient Transfer of Data

Efficient and timely transfer of data from the devices to the storage and analysis centre is another important research challenge. Very few works have been done in this research direction. Reliable delivery of data and Quality of Service plays a vital role in the success of the IoT system.

D. Mining of Required Data

Analysis of data and mining is a major task in IoT systems. With enormous amount of data accumulating every second it is a big challenge to classify the required and obsolete. Extracting the required information from this huge amount of data is a humongous task. Numerous researches are being carried out in this direction.

E. Visualization

Visualization is often a challenging task with enormous amount of data. Complexity reduction is another important research area with many opportunities. With type and size of data varying continuously from various devices and sources, it is often difficult to structure the collected data into a uniform schema.

V. Conclusion & Future Scope

In this article we introduced the subject of the distributed data analytics in the IoT network. We have seen extensive applications of Signal Processing in future IoT standards and in the emerging Smart Cities. The linear analytic models are well studied in the present literature, while non-linear analytics which are emerging in many IoT use cases, needs an emphasis. The physical layer communication protocols using energy harvesting methods are finding interest in many core researches in this area. The development of IoT network is dependent on the collaboration extended from various disciplines of Engineering. A realistic approach is one that unites with the existing Internet and other legacy technologies. We finally presented the open research problems in analytics of big data collected from IoT devices. This would definitely provide directions for research in this area in future.

In the near future, we present a novel architecture

cum working prototype of medical based device, which not manages big data efficiently but also highly secure and provides efficient data transfer from remote location to the centralized server.

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A Top-up Design for PAL to VGA Conversion in Real Time Video Processing System

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***Abstract*—Real time video processing found its range of applications from defence to consumer electronics for surveillance, video conferencing etc. With the advent of FPGAs, flexible Real-Time Video Processing System (RTVPS) which can meet hard real-time constraints are easily realised with short development time. A hardware software co-design for an FPGA based real time video processing system to convert video in standard PAL 576i format to standard video of VGA / SVGA format with little utilisation of resources is realised and evaluated. Switching between multiple video streams, character/ text overlaying, skin colour detection is also incorporated. The system is also adaptable for rugged applications. VHDL codes for the architecture were synthesized using ALTERA Quartus II and targeted for ALTERA STRATIX I FPGA. The evaluated results show that the resource utilization is low for this design. Since system is also flexible, latest applications can be incorporated in future.**

***Keywords*—FPGA, hardware software co-design, PAL, RTVPS, VGA/SVGA, VHDL**

I. INTRODUCTION

Nowadays digital information has become an inevitable part of our everyday lives in the form of digital audio, digital images, and more recently, digital video. Real-time digital video has found its applications in various fields like video conferencing, surveillance, medical imaging, remote vehicle guidance systems etc. Real time video processing system is very essential even in the field of defence for surveillance, various displays etc. Then along with functionality, the system must be rugged enough to operate in all environmental conditions. Special attention should be then given in hardware design to meet the requirements.

The concept of "real-time image processing" is defined as the "digital processing of an image which occurs seemingly immediately; without a user-perceivable calculation delay" [1]. Whether the Real-time video processing system does video filter or decode, encode, image transform or image compression and decompression or any video processing methods, it is mainly to complete the video signal acquisition, processing, storage and display, and the delay from the input time to output time must be small enough to meet the acceptable time value. Accuracy of the calculation depends not only on the results, but also on the time the output occurred [2].

In real time processing, specifications are very strict and are better met when implemented in hardware [3-5]. Features like potential of creating parallel processing architectures, embedded hardware multipliers, increased number of memory blocks, extremely high memory bandwidth enable video applications with FPGAs to outperform conventional DSPs [6]. They provide precise execution times helping to meet hard real-time deadlines. FPGAs can be configured to interface with various external devices. Since they are reprogrammable devices, they are flexible in the sense that they can be reconfigured to form a completely different circuit [1]. In RTVPS, a set of operations are repetitively performed on every image frame in a video stream. These operations are usually computationally intensive and, depending on the video resolution, can also be very data transfer dominated. These operations must be performed accurately and under real-time constraints as the results greatly affect the accuracy of application. Essential logic resources required in RTVPS operation are currently available optimized and embedded in modern FPGAs [8].

A Video Processing system with VGA interface is designed in [13]. Using the DSP + FPGA + SCM + ASIC architecture, it completes the acquisition of the video signal and display. Difficulty with this design is that its hardware dependency is more and use of special purpose chip would bring many problems such as design complexity, high cost and bulkiness. While in proposed design, FPGA is configured to perform all those functionalities achieved by different controllers in the previous design. In [2], a reasonable hardware and software division for the realization of the functions based on research of existing digital image processing algorithms is done. On this basis, an FPGA-based image processing system structure is developed, and respectively designs the structure of image acquisition and storage, image processing, real-time display and other functional modules. Difficulty with the design is that the whole preprocessing part is achieved by the custom hardware.

HDL is best suited for easy development of RTVPS where hardware platform of interest is FPGA. FPGAs allow

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fully application specific custom circuits to be designed by using hardware description language (HDL). For C, rapid development of algorithm is difficult. Usually the data-types used for variable declarations in C are not appropriate for real-time use. In many situations, floating-point data-types must be changed to appropriate integer data-types [1]. An efficient approach to design electronic devices is the high-level synthesis of behavior description captured at RTL level using HDL like VHDL. This technique finds great utilization in this era of Internet of Things [9-10] and fog computing [11-12] and highly dynamic ad hoc networks [13-14].

FPGA based system developed using HDL has more flexibility. ALTERA STRATIX I FPGA is used because the internal of FPGA has abundant triggers and I/O pins; the shortest design cycle, the lowest risk device; low power dissipation; compatible with CMOS or TTL level [16]. Industrial grade FPGA of this family is chosen to use so as to make the system adaptable for rugged applications. In the aspect of high-speed data acquisition, FPGA has incomparable advantages to single-chip microcomputer and DSP: the high clock frequency, small internal delay; internal logic all finished by hardware, high speed and efficiency; Flexible form, integrated peripheral control and interface circuit.

This paper is organized as follows: Section 2 defines the overview of the system. Section 3 explains the hardware software co-design implemented in the system. The experimental results and analysis of the design is presented in section 4, while concluding remarks and future work are given in section 5.

II. System Overview

This paper is based on the work done to develop an efficient method for converting video in standard PAL 576i format to standard video of VGA / SVGA format, in real time and is implemented in FPGA with little utilisation of resources, with VHDL used as the method of design entry for the entire system. The system has higher bandwidth to process video, enabling to switch fast between multiple video inputs and to buffer the real time video output that is to be displayed. Character/text overlaying and several other applications also have incorporated on the video. Block overview of the system developed is shown in Fig 1. Performance of a developed system greatly depends upon deciding which part of an application to be implemented in hardware or software. With increasing functions to be implemented in an embedded system always a hardware/software co-design is essential [17].

III. System Hardware Software Co-Design

Four modules present in a video processing system are video capture module, video control module, function expansion module and video display module.

A. Video Capture Module

Video Capture Module Hardware Diagram is shown in Figure 2. CCD camera (PAL) is used as the input video source. It captures video images, and then transmit back PAL format of the analog video signal for A / D conversion. PAL is 625 lines, 50 fields per second, 2:1 interlaced monochrome standard used in television broadcasting standard. At a time, up to 6 video inputs can be given to the system between which video switching is possible

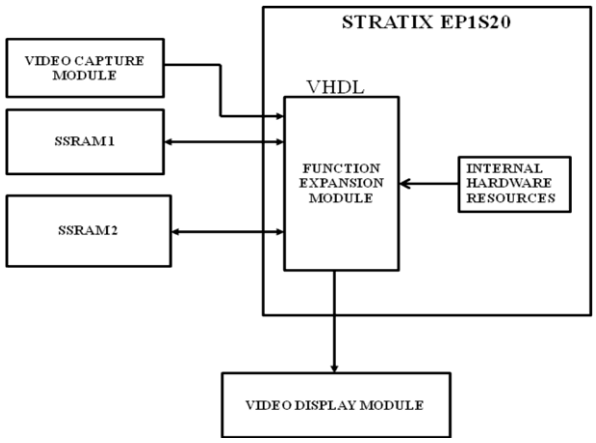

Fig. 1. System block overview

ADV7181 chip, a low power high speed multi-function digital video decoder chip is used in the system to complete the analog video signal to digital signal conversion. Along with decoding, video filtering should be done as part of image pre-processing. In the design of RTVPS proposed in [18], a chain of filters is incorporated along with other modules. The main problems in real-time video filtering are synchronization, memory usage and delay. They are directly related to cost of the filter [19]. With single ADV7181 chip it is possible to complete the video decoding along with all sorts of filtering; real-time video picture quality enhancement and its reliable control are possible

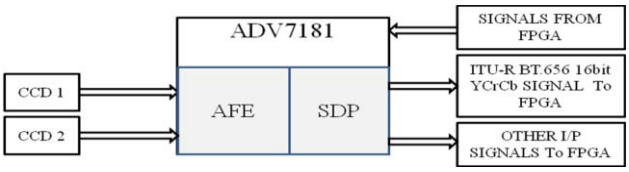

Fig. 2. Video capture module hardware diagram

B. Video Control Module and Video Memory

Real-time system needs to make a continuous and timely response to the environment which can be effectively achieved using FPGA and faster video memories. FPGA processes the received signal of YCbCr (4:2:2) format from the capture module. FPGA that used in the system is Stratix EP1S20 uses 1.5V power supply, 780-Pin FBGA package; the system uses an active crystal with 50MHz system working frequency. This module is always associated with a video memory. VGA display image data volume is usually huge, and with the built-in RAM blocks of FPGA, it is difficult to meet such a large amount of data, so there needs external RAM to store the data [20]. There are many choices for the external memory of FPGA, such as ROM, SRAM, SDRAM, FLASH etc. Developing efficient memory architecture would greatly improve memory accesses on FPGA and use of FPGA in RTVPS [17].

In this design two SSRAMs are used as video memories. SSRAM act as a buffer between the video capture and VGA display module that is, two systems with different speed. Synchronous pipelined burst SRAM (SSRAM) is SRAM

with burst read/write capability in linear or interleaved burst order. They are equipped with the advanced (NoBL) No Bus Latency logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This dramatically improves the throughput of data in systems that require frequent Write/Read transitions.

C. Video Display Module

This module is to real-timely convert the digital image the FPGA captured, into analog video data and output to the display with VGA interface. VGA (Video Graphics Array) is a video transmission standard that follows progressive scanning and has the advantages of high resolution, fast display speed and rich colour used in computer monitors [22].

D. Function Expansion Module

Different design modules that are designed, developed and implemented in FPGA, using VHDL to achieve system functionality are included in this module. This module is flexible. We can add, modify or adapt any features of the system in this module.

1) Configuration of Video Decoder: The ADC, ADV7181B requires a single 27 MHz clock which is provided from FPGA. ADV7181B should be configured accordingly the design demands. FPGA configure the decoder on the bus, using I2C protocol; 2-wire serial interface. Two signals, serial data (SDA) and serial clock (SCLK), carry information between the ADV7181B which act as a standard slave and the system I2C master controller FPGA. ADV7181B has 249 sub addresses to enable access to its internal registers, of which design need only 16 register configurations, the remaining registers are default values after the system reset. .

2) Colour Space Conversion: The Y-C component form is produced by phase- or frequency- modulating colour subcarrier(s) with the colour difference components, and then adding them together depending on which process is used. The Y signal represents brightness and the C signal represents colour. The colour-difference signals contain R (Red) minus the Y signal and B (Blue) minus the Y signal. YCbCr digital video according to BT.656 uses 4:2:2 sampling: Chroma samples are coincident (cosited) with alternate luma samples such as Cb, Y, Cr, Y, Cb, Y, Cr, etc. It specifies sampling of luma at 13.5 MHz and sampling of Cb and Cr colour difference components at 6.75 MHz. This interface is referred to as 4:2:2, since luma is sampled at four times 3.375 MHz, and each of the CB and CR components at twice 3.375 MHz – that is, the colour difference signals are horizontally sub sampled by a factor of 2:1 with respect to luma [7].

To transfer a television image to a computer monitor, we need to convert the image from the YCbCr colour space to the RGB colour space [23], [13]. Therefore, YCbCr data format from the decoder is converted into RGB format to display it in the computer monitor or LCD panel using the following conversion equation.

$$\begin{aligned} R &= 1.164(Y-16) + 1.596(Cr-128) \\ G &= 1.164(Y-16) - 0.813(Cr-128) - 0.391(Cb-128) \\ B &= 1.164(Y-16) + 2.018(Cb-128) \end{aligned} \quad (1)$$

3) Video Memory Buffering: The system uses 2 pieces of 1M x 24Bit SSRAM chip as the video memories to do ping pong buffering, where each memory need to perform only one memory operation per time slot; read and write operations can take place simultaneously in physically separate memory devices. The main benefit of a ping-pong buffer is that using conventional memory devices, it allows the design of buffers operating twice as fastwhich is the key of RTVPS [24]. The converted RGB data frame corresponding to the PAL interlaced format is written to memory1. For interlaced scanning, one frame is divided into two fields; odd field and even field. 720 active samples are present in each line in a frame. All the odd lines are allocated in the alternate 720 memory locations starting from base address, leaving space for the even field. For write operation, clock used is ADC output llc with which each line of PAL Video is sampled according to ITU-R_BT.656. While writing in memory1, reading is happening from memory2 in VGA progressive format. RGB data is read from continuous 640 memory locations by video display module starting from base address where the PAL data frames are stored. Memory architecture of the system is shown in Fig. 3. Once a frame has written to the memory, read and write operation is switched between the memories. Neither of the memory is doing same operation; while one frame is reading, next frame is writing simultaneously. It acts as interface between two different speed systems without delay

4)VGA Display Controller: FPGA reads out a line data from video memory of its party at first, sends them to the corresponding pixels on the monitor and then displays the next line. The next frame of image data will be displayed until all of above lines have been shown completely. In one second, the number of image frame demonstrated by a VGA monitor is the display refreshing rates. In a high enough refreshing rate, the human eyes will feel that the image is continuous, rather than be shown one line and line [21].

5) VGA/SVGA Display: VGA is the Video transmission standard defined in a range of resolution. Standard VGA resolution is 640x480, Super VGA resolution 800x600, Extended VGA resolution 1024 x 768 and so on. System is designed so as to display video either in 640x480 or 800x600. In both cases, pixel clock signal, Hsync, Vsync and blanking periods vary. To display in SVGA resolution any of the two simple methods could be used; Pixel duplication or nearest neighbor algorithm. For duplication, after each9pixel interval, RGB value of previous pixel is duplicated. Formally, to find a value for an output pixel located at (i, j), the nearest-neighbor method picks the value of the nearest input pixel to ((i+0.5) win/wout, (j+0.5) hin/hout). The calculation performed by the scaler is equivalent to the following integer calculation: $O(i, j) = F((2 \times win \times i + win)/(2 \times wout), (2 \times hin \times j + hin)/(2 \times hout))$. The calculation performed by the scaler is equivalent to the following integer calculation: $O(i, j) = F((2 \times win \times i + win)/(2 \times wout), (2 \times hin \times j + hin)/(2 \times hout))$.The width and height of the input image are denoted as win and hin respectively. The width and height of the output image are denoted as wout and hout. F is the function which returns an intensity value for a given point on the input image and O is the function which returns an intensity value on the output image [25].

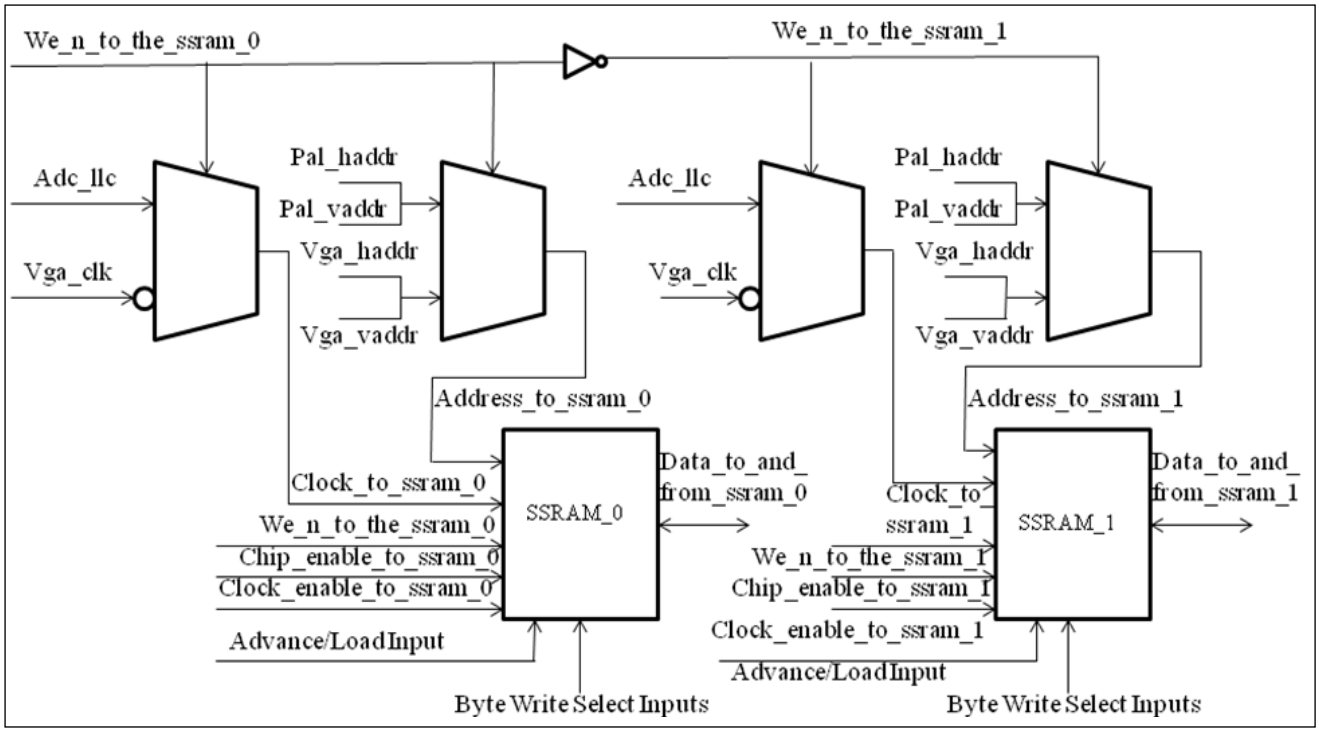

Fig. 3. Memory Architecure of the System

6) Skin Colour Detection: Real-time skin colour detection is one of the important research areas for automated video surveillance system. Skin colour detection in YCbCr colour space is chosen over RGB colour space. RGB model is not ideal since the red, green and blue colour components are highly correlated. Skin colour region is more effectively extracted in YCbCr colour space because Cb and Cr have some distinct colour range for skin region [26]. Thus algorithm works quite well. The skin colour detection condition for YCbCr colour space is given below [27].

$$Y > 60$$
$$85 < Cb < 135 \qquad (2)$$
$$135 < Cr < 180$$

The skin colour detection is performed on the video using YCbCr method and corresponding flag value is set to 1 or 0 based on skin pixel or non-skin pixel. Video output of the system employing skin colour detection.

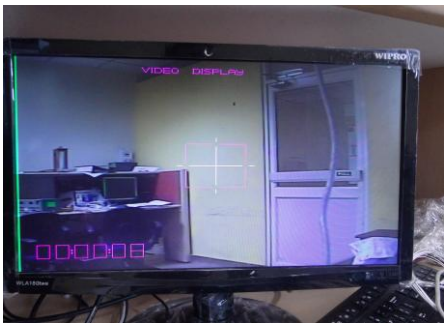

Fig. 4. A real time video output obtained by the system

IV. Implementation Results

The VHDL codes are synthesized using ALTERA Quartus II design software and targeted for Altera Stratix 1S20 FPGA. The software includes HDL and schematic design entry, compilation and logic synthesis, power analysis and advanced timing analysis, Signal Tap II logic analyser, and device configuration. After successful compilation programming file is downloaded to FPGA via a special circuitry and the associated software called as USB-Blaster which provides a Universal Serial Bus (USB) link to the host computer and JTAG UART interface to the board. The thermal power analysis results are presented in figure 5 and the resource utilization summary is presented in Table 1.The ALTERA Powerplay Power Analysis tools allow estimating device thermal power consumption. As design grow larger and process technology continues to shrink, power becomes an increasingly important design consideration. Thermal power is the power that dissipates as heat from the FPGA. The result of the Powerplay Power Analyzer is only an estimation of power. Summary of the analyzer by assuming default toggle rate of 12.5% for input signals is shown below. Total thermal power dissipation is estimated as 510.93mW. The static power is the thermal power dissipated on chip, independent of user clocks. Dynamic power is the additional power consumption of the device due to signal activity or toggling.

Total Thermal Power Dissipation	510.93 mW
Core Dynamic Thermal Power Dissipation	70.97 mW
Core Static Thermal Power Dissipation	359.91 mW
I/O Thermal Power Dissipation	80.05 mW

Fig. 5. Powerplay power analyser summary

TABLE I. RESOURCE UTILIZATION SUMMARY

	Resource	Usage
1	Total logic elements	1,995 / 18,460 (11 %)
1	-- Combinational with no register	1586
2	-- Register only	30
3	-- Combinational with a register	379
2		
3	Logic element usage by number of LUT inputs	
1	-- 4 input functions	1018
2	-- 3 input functions	457
3	-- 2 input functions	466
4	-- 1 input functions	23
5	-- 0 input functions	1
4		
5	Logic elements by mode	
1	-- normal mode	1460
2	-- arithmetic mode	535
3	-- qfbk mode	51
4	-- register cascade mode	0
5	-- synchronous clear/load mode	148
6	-- asynchronous clear/load mode	290
6		
7	Total registers	409 / 21,902 (2 %)
8	Total LABs	220 / 1,846 (12 %)
9	Logic elements in carry chains	587
10	User inserted logic elements	0
11	Virtual pins	0
12	I/O pins	205 / 587 (35 %)
1	-- Clock pins	2 / 16 (13 %)
13	Global signals	10
14	M512s	3 / 194 (2 %)
15	M4Ks	0 / 82 (0 %)
16	M-RAMs	0 / 2 (0 %)
17	Total memory bits	1,402 / 1,669,248 (< 1 %)
18	Total RAM block bits	1,728 / 1,669,248 (< 1 %)
19	DSP block 9-bit elements	0 / 80 (0 %)
20	PLLs	2 / 6 (33 %)
21	Global clocks	10 / 16 (63 %)
22	Regional clocks	0 / 16 (0 %)
23	Fast regional clocks	0 / 8 (0 %)

V. CONCLUSION

A novel real-time video processing system based on FPGA is developed for the efficient conversion of PAL to VGA, useful for rugged application with high bandwidth and little resource utilization. It can switch between multiple video input channels. Video output obtained is in real time and can display in VGA or SVGA format with character/text overlay. Entire functionalities and applications are developed using VHDL codes synthesized using ALTERA Quartus II design software and targeted for Altera Stratix 1S20 FPGA. The estimated FPGA resource requirements are reported. The design is flexible and is possible to broaden or add many applications in this design.

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Multi-Criteria Ranking of Best Management Practices for Flood Reduction in Kochi City, Kerala

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***Abstract*— This paper focuses on the flood management strategies which are appropriate for Kochi while considering water conservation aspects. Best Management Practices (BMP), the structural and non structural measures, to manage the quantity and improve the quality of storm water in cost effective manner were reviewed. The BMPs like permeable pavers, Rain barrels and infiltration trenches were analyzed for their hydrological performances using the Storm Water Management Model (SWMM) by US EPA. The present study applies a multi criteria analysis (MCA) namely analytical network process (ANP) to rank the BMPs for flood reduction in the city. MCA makes it possible to tradeoff various other criteria that can bring about sustainability element to the solution. The ranking was obtained considering multiple stakeholders like people, design engineers and policy makers.**

***Keywords*— Flood reduction, Best Management Practices, Multi Criteria Analysis, SWMM, Analytical network Process**

I. INTRODUCTION

Kochi, the most populated city in Kerala, is one of the 20 selected smart cities in India. The city is transforming from early-urban to middle urban stage [1]. Even at this growth stage, Kochi lacks sufficient drainage and sewerage system. The storm water in Kochi is managed through natural inland canals and secondary man made drains, constructed even without considering the actual runoff. Lack of sewerage network causes the households to use storm drains for sewage discharge thereby contaminating and clogging the drainage network of city. Any blockage in these open drains or canals results in inundation of the surrounding area with sewage mixed storm water. On the other side, the city is under acute water scarcity due to contaminated ground water and mostly unreliable and insufficient supply through pubic distribution network [2]. Therefore, managing large volume of storm water without flooding while utilizing it as a resource to enhance urban water security is of prime importance to Kochi.

The present work evaluated some of the Best Management Practices (BMP) [3] for storm water management such as rain barrels, infiltration trench, pervious pavements and permeable interlocking pavements. A ranking of BMPs or their combinations were carried out using multi-criteria analysis (MCA) based on technical, social, economic and environmental criteria with focus on flood reduction and harvesting of rainwater in the urban area.

II. STUDY AREA

49 sq. km of eastern Kochi divided into 137 sub catchments was considered in the present study. Catchments were selected such that they are bounded by water bodies on all sides. Overflow effects from the upper catchments are therefore avoided in such hydrologically isolated catchments. The study area and the catchment subdivision are given in figure 1. A drainage map of the study area, was prepared from the ground contour (created using SRTM- DEM) and inland water way map, as shown in figure 2.

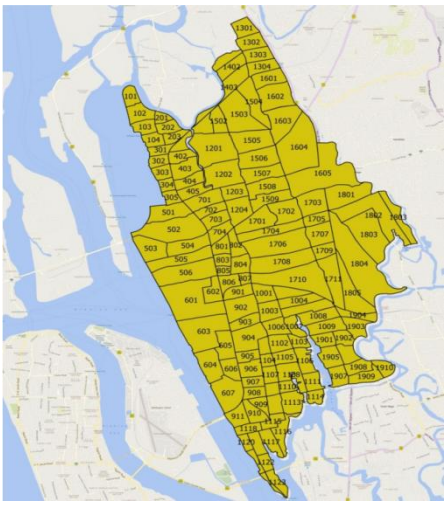

Figure 1 - Catchment area and its subdivisions.

Figure 2 also shows problematic area with 500 m buffer zone created for finding out the weightage factor for problematic area nearness. The nodes coming under these buffer zones are more significant in causing flood problems to the public compared to the other areas.