B

06EC6025 **Reg. No _____**

Name _____

A P J ABDUL KALAM TECHNOLOGICAL UNIVERSITY

M.TECH DEGREE EXAMINATION, DECEMBER 2017

FIRST SEMESTER

Branch: VLSI & Embedded Systems

Analog Integrated Circuit Design- I

Time: 3 Hours **Max. Marks: 60**

PART A

Answer ALL questions

1. Explain the small signal capacitance of a two terminal of a MOS structure.
2. With suitable diagrams, explain the working of 4 terminal MOS device.
3. The effect of DIBL and velocity saturation becomes significant only in MOS transistors having channel length less than 180nm. Justify this statement.
4. For the amplifier circuit shown in fig.1 find the maximum output voltage swing

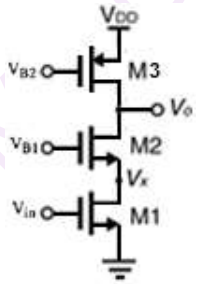

Fig. 1

(4 x 5 marks =20 marks)

PART B

5. (a) Obtain an expression for flat band voltage of a two terminal MOS structure using potential and charge balance equations. [6]

   (b) Calculate the flat-band voltage for a two terminal MOS structure with n-type substrate with $N_D=10^{17}/cm^3$, SiO_2 insulator with $\mathbf{t_{ox}}$ = 60 Å, and Al gate. The contact potential between Al and intrinsic Si is 0.6V. The interface charge

density, $Q_o' = 5x10^{-8}$ C/cm^2. [k=8.62x10^{-5}eV/K, $\epsilon_0 = 8.854x10^{-14}$ F/cm, n_i for Si = 1.5 x 10^{10}/ cm^3, $\epsilon_{SiO2} = 3.9$, $\epsilon_{Si} = 11.9$] [4]

OR

6. With the help of energy band diagram, discuss the effect of gate substrate voltage on surface charge and surface potential

7. Derive the current equations of a 4 terminal MOS transistor using Complete All Region Model. Also obtain current equations using charge sheet assumption.

OR

8. For a 4 Terminal MOS structure, with the help of suitable derivations explain the simplified symmetric strong inversion model. Using Simplified Source-referenced Strong Inversion model, derive the expressions for Drain to source current in Triode and Saturation region of operation?(assume $\alpha=1$, $\gamma=1$)

9. (a)Explain the significance of input referred noise in the case of common source amplifier. [4]

   (b)Derive the expression for input referred noise for the circuit shown in fig.2. The circuit is affected by thermal and flicker noise. [6]

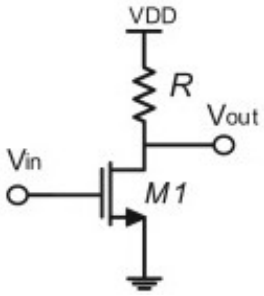

Fig. 2

OR

10. (a) Estimate the effect of scaling on channel capacitance and S/D junction capacitance of a MOSFET [4]

    (b)Show that scaling improves the performance indices- speed, power and size- of MOS circuits [6]

11. (a)Derive the small signal gain of the common source amplifier with diode connected load and current source load. [8]

(b) Discuss the need of a degeneration resistor at the source? What is its effect in the circuit? [2]

OR

12. Point out the advantages of folded cascode amplifiers over cascode amplifiers. Derive an expression for small signal gain of the amplifier shown in fig.3.

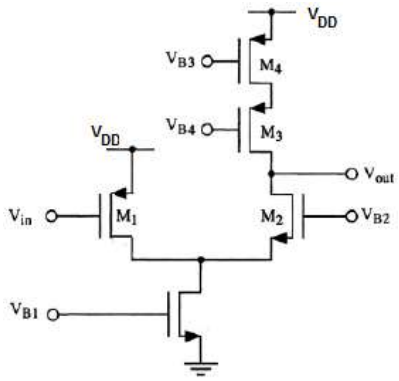

Fig. 3

(4 x 10 marks =40 marks)