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06EC6015 **Reg. No _____**

Name _____

A P J ABDUL KALAM TECHNOLOGICAL UNIVERSITY

M.TECH DEGREE EXAMINATION, DECEMBER 2017

FIRST SEMESTER

Branch: VLSI & Embedded Systems

CMOS Digital Design

Time: 3 Hours **Max. Marks: 60**

PART A

Answer ALL questions

1. Give a comparison between NMOS , pseudo NMOS and CMOS logic with help of a suitable example
2. Illustrate the solution of the monotonicity problem in dynamic logic using Domino CMOS.
3. Explain klass SD flip flop?
4. Explain the operation of 6T SRAM cell.

(4 x 5 marks =20 marks)

PART B

5. (a) Draw the voltage transfer characteristic (VTC) curve of a CMOS inverter and identify the regions of operation of the transistors corresponding to the regions in the VTC. Assume that the transistors are having symmetrical rise and fall times and operating at 3.2 V. Threshold voltage is Vtn=|Vtp|=0.7 V. [5]

   (b) Calculate the switching threshold of a CMOS inverter with following parameters:

   V_{DD}=5 V, V_{tn}=0.4 V, V_{tp}=-0.4 V, β_n=50 μA/V^2, β_p=25 μA/V^2. Whether the inverter is HIGH skewed or LOW skewed? [5]

OR

6. (a) Explain on different Interconnect impacts in a VLSI circuit with relevant equations. [5]

   (b) How cross talk effects are controlled in interconnect engineering? [5]

7. (a) Describe the working of pass transistor circuits. [5]

   (b) Explain charge sharing and charge leakage in dynamic circuits. [5]

OR

8. (a) Describe with necessary diagrams MODL and NP-Domino Logic. [6]

   (b) Explain the working of BiCMOS circuits with a suitable example. [4]

9. Discuss the maximum and minimum delay constraints concept in flip flops, two phase latches and pulsed latches sequencing styles?

OR

10. (a) Discuss global clock generation scheme in a chip? [6]

    (b).Briefly explain the working of simple synchronizer? [4]

11. Draw the configuration of a square root carry select adder and mark its worst case signal arrival time. What are its advantages? Also obtain an expression for its propagation delay.

OR

12. Draw the composition of a 4 x 4 bit array multiplier for unsigned numbers. Also obtain an expression for its propagation delay.

(4 x 10 marks =40 marks)