Vidya Nagar, Karukutty - 683 576 Time Table w.e.f. 17-07-2024

ELECTRONICS & COMMUNICATION ENGINEERING (S5) - Class Room AC 1 202

			RONICS & COMMUI		ERING (55) -	1.05-1.55 pm	2.05 -2.55 pm	2.55 - 3.45 pm		
Day	8.45 - 9.35 am	9.35 - 10.25 am	10.35 - 11.30 am	11.30 -12.20 pm		1.05-1.55 pm	0.000			
Mon.	MINOR/CS(R)	AIC (F	(S\CS)		LIC	DM	ADC(T)			
Tue	LIC	cs	DSP	IEFT	LUNCH	DM	CS	LIC(T)		
Wed	MINOR/(DSP(R)		ADC	DM	BREAK	CS	DSP(T)	IEFT		
	and the second control of the second control		CS	LIC		AIC (RG*,CJ)/DSP Lab (SV*,CD)				
Thu	ADC	DSP		DSP		ADC	DSP	CS(T)		
Fri	MINOR(LIC)	IEFT	ADC	DOP						
	urse Code	·	Course Name				ne of Faculty			
	ECT 301					Ms Retty George, Ms Neethu Susan Idikulay				
LIC					AV,SAJ	Ms.Anandhi V,Dr Sreeja KA				
DSP	ECT 303	Digital Signal Processing			DKS,LNM	Dr Deepak KS ,Ms Lekshmi Nair M				
ADC	ECT 305		Analog and Digital Communication			Mr Ajit Joseph, Ms Sandhya Venugopal				
CS	ECT 307	Control Systems	Control Systems			Mr.Akhil Baby Thomas				
IEF	HUT300		Industrial Economics & Foreign Trade Disaster Management			Ms Neethu Susan Idikulay				
DM	MCN301				NSI	Ms Retty George				
AIC LAB	ECL 331	Analog Integrate	d Circuits and Simula	ation Lab	RG*,CJ SV*,CD	Mis Relly George	ugopal*,Ms Chaitar	va Das Nithin		
SP LAB	DESCRIPTION OF SHAPE		Digital Signal Processing Lab					i,a dat i		
	CST-383		Concepts in Machine learning			Ms.Aiswarya Me	11011			
R/M	001-500	Honours Course								
HON		Minor Course				-	7			
MIN	DEM	Remedial								
REM	REM	\ \				1.m				

HOD DEPAM

PRINCIPAL

Vision of the Department	
1	M1 Impart a solid foundation in the field of Electronics and Communication. M2 Provide education with emphasis on the ethics, leadership, and entrepreneurship necessary for students to become successful contributors to society. M3 To create individuals who can continue to learn on their own to scale greater heights in their profession.

Vidya Nagar, Karukutty - 683 576 Time Table w.e.f. 17-07-2024

ELECTRONICS & COMMUNICATION ENGINEERING (S7) - Class Room No.AC1 201

Day	8.45 - 9.45 am	9.45 - 10.45 am	11am - 12pm		12.45-1.40 pm	1.40 -2.35 pm	2.50 - 3.45 pm	
Mon.	MAC	ISE	OE	1	EMS LAB (AJ*,NM) /SEM (PM*,AV)			
Tue	OFC	ISE	OFC	LUNCH	MAC	ISE	OE	
Wed		EMS LAB (AJ*,NM) /SEM (PM*,AV)			OE	MAC	OFC(T)	
Thu	OE	OFC	MAC	1	ISE	OFC	MAC(T)	
Fri	1 01	PROJECT(LNM*,V	1570511305-	1	PROJECT(LNM*,VPG)			

		Course Name		Name of Faculty	
Course	e Code		SSM,DKS	Ms Sukanya Singh M J ,Dr Deepak KS	
MAC	ECT401	Microwaves and Antennas		Mr Vinoj P G,Ms Praveena S Kammath	
OFC	ECT413	Optical Fibre Communication	VPG,PSK		
0.0		Natural Disasters and Mitigation	PAV	Dr. Praseeja A V	
OE	CET 445		DJY	Ms.Deepa Johny	
	CST 445	Python for engineers		Ms Lekshmi Nair M	
ISE	MCN401	Industrial Safety Engineering			
	A Principle of the Control of the Co	Electromagnetics Lab	AJ*,NM	Mr Ajit Joseph* ,Ms Nithya M	
EMS Lab	ECL411		PM*,AV	Dr.Parvathy.M*,Ms Anandhi.V	
SEM	ECQ413	Seminar	LNM*,VPG	Ms Lekshmi Nair M*, Mr Vinoj P G	
PP-1	ECD415	Project Phase I	LININ , VI O	INIO ZONO.	

Principal

Vision of the Department	To achieve academic excellence in Electronics and Communication Engineering and mould technically competent engineers by imparting quality education to the students while keeping in tune with the ever-changing industrial demands and societal needs.
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Vidya Nagar, Karukutty - 683 576

Time Table w.e.f 17-07-2024

BTECH IN ELECTRONICS ENGINEERING(VLSI DESIGN AND TECHNOLOGY) (S3) - Class Room No.AC I 205

	BILO	THE ELECTROTHE	S ENGINEERING(VI	1	4	5	6	7		
	11	2	3	-	12.15 -1.05pm	1.05-1.55 pm	2.05 -2.55 pm	2.55 - 3.45 pm		
Day	8.45 -9.35 am	9.35 -10.25 am	10.35 -11.30 am	4		SE SE	NT	LCD		
Mon.	SSD	DE	PDECA	LUNCH	LCD	LCD(T)	Y2P	PDECA		
Tue	NT	PDECA	SSD	BREAK	NT (R)		DE	NT(T)		
Wed	LCD	NT	SE		PDECA(R)	LCD Lab (SAJ*,VVG)				
Thu	PDECA	LCD	SSD(T)		SSD(R)		PDECA	SSD		
Fri	15257.	SCL Lab (AV*,S	V)		LCD(R)		NI IDEO.			
	Codo		Course Name			Name o	f Faculty			
Co	urse Code	D. II I D'II tio		Analysis	RR	RR Mr Rahul Ravi				
PDECA	MAT201	Partial Differential Equation & Complex Analysis			PM,SMJ	Dr.Parvathy.M,Ms Sukanya Singh MJ				
SSD	ECT201	Solid State Devices			SAJ,AJ	Dr.Sreeja K A,Mr Ajit Joseph				
LCD	ECT203	Logic Circuit Design				Ms Chaitanya Das Nithin,Ms Anandhi V				
	ECT205	Network theory			CD,AV					
NT			nooring		WG	Ms Vrinda. V. Gopal T				
DE	EST200	Design and Engineering			SV	Ms Sandhya Venugopal				
SE	MCN201	Sustainable Engi	ineering			Ms Anandhi.V*,Ms Sandhya Venugopal				
	ECL201	Scientific Compu	iting Lab		AV*,SV	Dr.Sreeja K A*,Ms Vrinda V Gopal T				
SCL LAB		Logic Design La			SAJ*,VVG					
LCD LAB					SSA	Ms.Shali Sara Abrah	idili			
MIN	CST283	Python for machine learning								
R	REM		Remedial			Mrs. Rony Tresa Da	IVIS			
V2P		Youth to Power	nday to Friday) and will b	o intimated we	Il in advance.	1.hr	_/			

PRINCIPAL

HOD	5 viscosing and mould technically competent engineers by
Vision of the Department	To achieve academic excellence in Electronics and Communication Engineering and mould technically competent engineers by imparting quality education to the students while keeping in tune with the ever-changing industrial demands and societal needs.
	M1 Impart a solid foundation in the field of Electronics and Communication. M2 Provide education with emphasis on the ethics, leadership, and entrepreneurship necessary for students to become
Mission of the Department	M2 Provide education with emphasis on the successful contributors to society. Successful contributors to society. M3 To create individuals who can continue to learn on their own to scale greater heights in their profession.
	M3 To create members

Vidya Nagar, Karukutty - 683 576

Time Table w.e.f 17-07-2024

ELECTRONICS & COMMUNICATION ENGINEERING (S3) - Class Room No.AC I 206

		ELECTRONIC	S & COMMUNICATION E	NGINEERING	1 (33) - Class IX	5	6	7
	1	2	3		4		2.05 -2.55 pm	2.55 - 3.45 pm
Day	8.45 -9.35 am	9.35 -10.25 am	10.35 -11.30 am		12.15 -1.05pm	1.05-1.55 pm	PDECA	SSD
Mon.	SE	SSD	PDECA	LUNCH	NT	DE		SE
Tue		(SSM*,NSI)/LCDL	ab (MC*,PSK)	BREAK	NT(R)	LCD	NT(T)	SSD(T)
	PDECA	DE	Y2P	- BREAK	SSD(R)	PDECA	LCD	
Wed		NT	SSD		PDECA(R)	NT	SSD	LCD
Thu	LCD		LCD(T)		LCD(R)	SCL (SSM*,NSI) /LCD Lab (MC*		ab (MC*,PSK)
Fri	NT	, 525,				Name of Faculty		
Cou	rse Code		Course Name			Dr. Nuja Unnikr	ishnan	
PDECA	MAT201	Partial Differential Equation & Complex Analysis				Mr Dinesh Babu ,Dr Parvathy M		
SSD	ECT201	Solid State Devices				Ms Nithya M,Ms Vrinda V Gopal T		
LCD	ECT203	Logic Circuit Design	Logic Circuit Design			Ms Praveena S kammath, Ms Retty George		
NT	ECT205	Network theory					Kammaur, wis Nei	ity deolige
DE	EST200	Design and Engine	ering			Mr Vinoj PG		
SE	MCN201	Sustainable Engine			SAJ SSM*,NSI	Dr Sreeja KA Ms Sukanya Singh M J*, Ms. Neethu Susan Idicu		
SC LAB	ECL201	Scientific Computin	Scientific Computing Lab			Ms Mary Catherine V G *,Ms Praveena S kammal		
LCD LAB	ECL203	Logic Design Lab			in the standard of the section of			
MIN	CST283	Python for machine	learning		SSA	Ms.Shali Sara A	oranam	
R	REM	Remedial				M. Jana Thora		
Y2P	, acm	Youth to Power	-		JT	Ms. Jane There	Sa	

Saturday's Time table will be on a rotation basis (Monday to Friday) and will be intimated well in advance.

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PRINCIPAL

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